(2)

SEMIANNUAL REPORT-

AN ACOUSTIC CHARGE TRANSPORT IMAGER FOR HIGH DEFINITION TELEVISION APPLICATION

W. D. Hunt, K. F. Brennan, A. Torabi, and C. J. Summers
Georgia Institute of Technology
Atlanta, Georgia
30332-0250

Contract # ?

92-1902

Executive Summary: Semiannual Report -

An Acoustic Charge Transport Imager For High Definition Television Applications

W. D. Hunt, K. F. Brennan, A. Torabi, and C. J. Summers
Georgia Institute of Technology
Atlanta, Georgia
30332-0250

Enclosed is a full report covering the first six months of work on the DARPA sponsored project, "An acoustic charge transport imager for high definition television applications". Here, we present a short, executive summary highlighting the accomplishments discussed within the enclosed semiannual report.

The primary goal of this research is to demonstrate the feasibility of developing an acoustic charge transport (ACT) imager for high definition systems applications. The operation of the proposed camera chip can be subdivided into three distinct functions; image capture, charge collection and storage, and charge readout for image reconstruction. The image capture stage of the device will be a GaAs/AlGaAs multiple quantum well avalanche photodiode (APD). Following the APD device is a charge storage and overflow heterostructure transistor which controls charge transfer into the ACT channel for readout and processing. In the enclosed report we discuss progress towards developing each of these three aspects of the chip as well as work towards integrating these components into a successful working device.

Theoretical and experimental work done to date have determined that a GaAs/AlGaAs APD structure can deliver a gain of ~ 5 at an excess noise factor of ~ 1.6. This is the lowest noise operation ever reported for a compound semiconductor APD device. Though the structures studied experimentally do not presently exhibit adequate gain/noise performance

for HDTV applications, theoretical studies indicate that the chosen APD design can ultimately meet the required specifications. It should be further emphasized that the current experimental results are close to the desired specifications, though further experimental and theoretical work needs to be done in order to develop a successful device. Specifically, the doping concentrations within the APD structures must be controlled to within $\sim 0.1\%$ of the desired values. This requires some improvement in precision doping techniques and control of material quality which we are pursuing.

Preliminary work has been done on the design of the charge transfer and collection transistor. We are currently developing an extensive theoretical analysis based on the self-consistent solution of the Poisson and drift-diffusion equations for designing the overflow transistor. At the present time, we have developed a simple prototype structure which we intend to grow and fabricate in our laboratory. Successful performance of the transistor depends upon improving material and surface quality. We have explored various new approaches to improve our growth techniques. These include modification of the Ga source, utilization of a class 10 glove box attached to the wafer entry chamber of the MBE system, and an indium free wafer holder.

Finally, we have made significant progress towards the development of high frequency ACT readout devices. Extensive theoretical work has been performed on the development of a computational means of determining the electric potential propagating with a surface acoustic wave. Based on this work, and study of waveguide mode profiles, we have designed ACT structures and have laid out and ordered mask sets for the first set of ACT devices to be grown in the laboratory. In addition, we have designed a mask for material studies that will enable the evaluation of the material grown for the APD and ACT devices as

well as enable us to monitor any alterations in material quality that may occur as a result of the fabrication procedures.

In summary, though much work needs to be done, we are confident that the proposed device design will ultimately deliver performance acceptable for HDTV applications.

AN ACOUSTIC CHARGE TRANSPORT IMAGER FOR HIGH DEFINITION TELEVISION APPLICATIONS:

SEMIANNUAL REPORT

William D. Hunt,

Kevin F. Brennan,

School of Electrical Engineering

and

Abbas Torabi,

Christopher J. Summers

Georgia Tech Research Institute

Georgia Institute of Technology,

Atlanta, Georgia

30332

In this report, we briefly describe the progress made to date towards the development of a new, high definition television camera chip utilizing an acoustic charge readout scheme. The design can be subdivided into three separate components, an avalanche photodiode, charge transfer and collection transistor, and an acoustic charge transport readout stage. Progress has been made in the design and analysis of each of these component parts. In Section I of this report, we describe the work accomplished to date on the development of an acoustic charge readout device. The theoretical work is described in Section II while the progress on materials growth is reviewed in Section III.

I. Work accomplished to date: Acoustic charge transport devices.

1. Development of software to compute the electric potential propagating with a surface acoustic wave (SAW) device propagating in a multilayered substrate:

In the development of the optimal architecture for the ACT imager chip it is imperative that we be able to predict the profile of the electric potential propagating with the surface acoustic wave. As is the case for most devices fabricated on a GaAs substrate we can engineer the device material using an epitaxial crystal growth technique such as molecular beam epitaxy (MBE). This provides us with a great deal of flexibility in the device design but it also presents us with challenges in our efforts to predict the operation of the device and subsequently optimize performance.

We are principally interested in predicting the magnitude and shape of this profile at the depth in the substrate where the charge is to be transported. To this end we have developed a computer program which will compute this potential program for an arbitrary multilayered structure where the layers may be of distinctly different materials. The program takes as input the material, type, thickness, crystal cut and acoustic propagation direction of the various layers within the structure and predicts the SAW velocity, piezoelectric coupling constant, the acoustic field profiles and the electric potential profile. At the present time we can compute these attributes for both metallized (short-circuit) and unmetallized (open-circuit) surface conditions and will be extending this technique to treat surfaces with

conductors of arbitrary resistance.

We have used the technique to predict the enhancement which could be achieved with thin film piezoelectric overlays such as ZnO, PZT, $BaTiO_3$, $PbTiO_3$ and AlN over a GaAs/AlGaAs heterostructure suitable for acoustic charge transport [1]. It was found that ZnO would be the best thin film choice from strictly an acoustic perspective and that a ZnO film of .3 to .5 acoustic wavelengths thick would, for a given RF drive level to an interdigitated transducer, increase the electric potential at the transport depth by a factor of 7 to 9 over what it is for a conventional heterostructure ACT device. This would result in a 17 to 19dB reduction in the RF drive power required for charge transport. A lower RF drive power in turn results in the obvious reduction in chip power consumption and the concomitant increased lifetime and reliability of the device. Again, this analysis tool will help considerably as we seek to establish the optimum device design.

2. Development of stack matrix theory software to compute waveguide mode profiles:

Acoustically the ACT imager can be thought of as strips of fast and slow regions regardless of the final form of the device architecture. As such we can view the imager area as an array of acoustic waveguides and we have developed an analytical tool based on stack matrix theory from integrated optics to predict acoustic beam profiles in complex waveguide array structures. This program allows the user to evaluate an arbitrary arrangement of acoustic waveguides with complete flexibility as to the proximity and size of the waveguides

as well as the acoustic velocity within the waveguides and the acoustic velocity in the regions between the waveguides.

This tool has already been experimentally verified [2] for SAW resonator devices which are to be utilized by Bell Northern Research (BNR) for microwave radio telecommunications. The agreement between theory and experiment is exceptionally good. We firmly believe that we have developed a technique which will give us accurate predictions about the acoustic beam profile in the imager region of our chip. BNR anticipates that its business will grow considerably in this area and the design tool we have developed is a part of their effort by way of research funding we are currently receiving from BNR.

3. Cell architecture design:

We continued to refine our cell architecture. Our current approach assumes that we begin with a GaAs substrate and grow the layers associated with the superlattice avalanche photodiode, the ACT channel and any thin film piezoelectric overlay on that substrate. The appropriate photolithography and etch steps will then be performed so that ion implantation can be used to impose channel stops to isolate the columns of the imager array and provide a mechanism for excess charge to bleed off. We will in the coming months be working with the theoretical group to hone this architecture and will also work closely with the fabrication and materials group to ensure that the architecture chosen is a manufacturable one.

4. ACT devices:

We have designed the mask for the first round of ACT devices and should receive the mask set within the next few weeks. This design includes delay line as well as RF analog memory devices. With these devices we will be able to investigate the charge transfer efficiency and noise characteristics for a multitude of material designs, thus enabling us to discern the optimal architecture from an experimental standpoint. In addition, we will be able to investigate the attributes of charge transport in a standing wave. The ultimate goal of this aspect of the program is to establish the optimal device architecture for the ACT portion of the imager chip. Along the way will be developing experimentally verified design tools which will allow us to fine tune the architecture for maximum signal to noise ratio and array uniformity. We have also established the fabrication parameters and procedures for the ACT devices and will continue to work towards solidifying these procedures in a way that resembles an industrial foundry process.

5. Mask design for material test devices:

In cooperation with Dr. Chris Summers we have designed a mask for material studies that will allow us to evaluate the material grown for the APD and the ACT devices but will also allow us to monitor any alterations in material quality that may occur as a result of the fabrication procedures associated with the imager chip. Spatial uniformity across the chip is of the utmost importance in the eventual HDTV camera chip and these material test devices

will allow us to monitor our processes in detail and to determine what procedures, if any, impact the achievable uniformity of the chip.

II. Work accomplished to date: Theoretical program

The theoretical program during the first six months has concentrated on studying the performance of the APDs and the charge transfer, collection transistor. The optimal performance of the doped well and doped barrier APDs, assuming "ideal conditions", i.e., absence of interface states, Auger recombination, deep level traps, and total depletion of each p-i-n layer, has been accomplished. It has been determined that very high gain, $\sim 10^4$, at an excess noise factor of less than 2, can be attained in either design using GaAs/AlGaAs. Comparison to existing HDTV camera devices indicates that this predicted performance far exceeds that of either the HARPICON H4318 tube camera or the amorphous silicon overlaid CCD camera. The existing cameras exhibit $\sim$ 70 dB signal-to-noise ratio which is consistent with a gain of $\sim$33 at an excess noise factor of $\sim$2.5. Therefore, if optimal performance can be achieved, the doped well and barrier devices will deliver more than adequate performance.

Experimental results indicate that the doped well design is easier to realize than the doped barrier design since the doping concentrations can be more readily controlled in GaAs. Nevertheless, there is some difficulty in achieving better than 0.1 % matching in doping concentration between the p and n layers in either case. Full depletion of each stage in a multistage structure is hence unlikely leading to fewer operating stages in the device. As a

result, the actual gain that can be attained at a low multiplication noise may be far lower than that predicted assuming full depletion as discussed above. An alternative strategy is to utilize lower doping concentrations within each unit cell to ensure nearly complete depletion of the structure. Presently, we are recalculating the gain, noise factor and bandwidth for modified GaAs/AlGaAs structures in which the doping concentration is reduced by an order of magnitude from that done previously. This will determine whether acceptable APD performance, as measured by the gain and noise, can be achieved utilizing the existing device design and growth capability.

Additional progress has been made towards improving the accuracy of the APD model. A much more realistic treatment of the impact ionization transition rate in GaAs has been developed in which the k-dependence of the impact ionization rate is included. We have found that the ionization rate is highly k-dependent and should be included in studies of the ionization rate. The details of this study are discussed in reference [3]. We are also currently revising our existing hole simulator code to properly take into account the k-dependence of the impact ionization rate as well as the warping of the valence bands with increasing energy. With these changes, a far more accurate assessment of the impact ionization rates and equivalently the gain, noise and bandwidth, of the doped well APD structures can be achieved.

The study of the charge transfer, collection and overflow transistor requires the development of a 2-3 dimensional Poisson solver coupled with the drift-diffusion equations. We have developed a 2-dimensional solver and are currently extending it to three dimensions. This model enables the examination of the performance of various device

designs. Given specified doping concentrations, layer widths, and biases, the conduction band bending can be ascertained and in turn, the charge capacity and leakage currents can be determined. To date, we have examined a representative n-p-n charge overflow transistor using the two-dimensional solver. It is found that a suitably deep collection well can be created while a charge overflow and charge transfer mechanism can be produced.

III. Work accomplished to date: Material growth program

In this section we briefly describe the progress made towards developing the three critical device structures required for this program: the multiple quantum well (MQW) avalanche photodiode, the acoustic charge transport device and the charge transfer device. We will also discuss the advances undertaken in materials growth to achieve high performance structures.

1. Avalanche photodiode studies:

A study has been completed on doped barrier AlGaAs/GaAs MQW-APD structures [4]. This study demonstrated the high potential of this device concept and also suggested new structures and techniques to be investigated. A practical limitation of these structures was found to be the need to obtain very precisely matched n- and p-type doping in order to achieve an exactly compensated or fully depleted mini p-n junction. When doping at the 1-5x10^{18}cm^{-3} level a small imbalance in p- and n- type doping levels of 1 to 10% results in a residual or background carrier concentration of 1x10^{16} - 1x10^{17}cm^{-3} in the gain or depletion

region of the device. This makes it impossible to fully deplete a 2-3μm thick structure with 20-25 gain stages. For this reason we have investigated the doped quantum well (QW) devices with slightly lower doping levels, different gain stages, and also with slight variations in doping concentration and position. The latter variation being to investigate the effect of diffusion in the structure.

In the first set of experiments a 300Å wide region in the QWs was doped; 150Å with Si (n doping) next to a 150Å region of Be (p doping). The Al mole fraction in the barriers was kept at 43% as a result of our prior experiments. The QWs were doped at concentrations of either $1.1x10^{18}cm^{-3}$ $5.05x10^{17}cm^{-3}$. This should change the field strength in the QW region by a factor of 2, thus producing a variation in the impact ionization values.

The second variation was to increase the number of superlattice periods from 5 to 10, 15 and 25. This would allow us to observe how many unit cells are contributing to the impact ionization process. If the doping was perfectly balanced then all the cells would contribute to gain and an increase should be observed in the APDs with larger number of unit cells.

In the next set of experiments the doping concentration of one of the species in the quantum wells was bracketed at 10% and 20% above and below the required doping concentration needed to obtain exact compensation. These experiments were designed to allow us to compensate for any doping imbalances.

Finally to investigate the possibility of dopant diffusion from the quantum well into the AlGaAs barrier, a 34Å or 70Å spacer layer of intrinsic GaAs was placed between the doped layers and the barriers. From other studies we have learned that Be diffuses faster

than Si in GaAs. Thus the diffusion of Be which is located closest to the AlGaAs barrier could cause a dopant imbalance within the QWs. Tables 1 and 2 list the APD growth runs performed with respective parameters for each structure.

To date a complete set of experiments has been performed on the first set of conventionally doped QW MQW-APD devices.

Gains up to 400 have been observed for bias voltages up to 12 volts. Note that the bias voltages are slightly higher than the doped barrier devices because of the lower doping used. The dependence of the multiplication excess-noise factor on gain is shown in Figure 1 for a ten period device. The electron to hole ionization ratio, $k_{eff} = \alpha/\beta$, is between 10 and 33 for low gains, but decreases for gains higher than 5 to approximately 5. These results confirm that at low bias voltages the built-in field due to the doping produces lower noise and that for higher bias voltages the applied field makes the electron and hole ionizations more equal.

Currently several other APD designs are in the fabrication process and will be characterized within the next two months.

As a summary of the AlGaAs/GaAs MQW-APD structures performed to date we tabulate in Table 3 the performance specifications achieved for the MQW-APD, the doped barrier APD and the doped Quantum Well MQW-APD. Note the superior performance of the doped structures with lower bias voltage, higher gain, and lower excess-noise than the undoped conventional MQW-APDs. The doped QW device also shows the highest gain, but has a noise figure similar to the doped barrier APD. As described previously more data will soon be available to investigate this point.

Table 1. Superlattice APD structures grown.

RUN #	L_b(A)	L_a(A)	Doping $10e^{17}cm^{-3}$	Doping width(Å)	%Al Composition	Periods
B91-75	500	500	0	0	55	25
B91-76	800	200	0	0	43	10
B91-77	500	500	0	0	43	10
B91-78	500	200+150+150	11	150	43	5
B91-79	500	200+150+150	11	150	43	25
B91-80	500	200+150+150	11	150	43	10
B91-81	500	200+150+150	11	150	43	15
B91-82	500	200+150+150	5.05	150	43	25
B91-83	500	200+150+150	5.05	150	43	15
B91-85	500	200+150+150	5.05	150	43	10
B91-86	500	200+150+150	5.05	150	43	5
B91-87	0	700+150+150	5.05	150	0	15
B91-88	0	700+150+150	5.05	150	0	10
B91-89	0	700+150+150	5.05	150	0	15
B91-91	500	700+150+150	11	150	0	10
B91-96	500	200+150+150	12.1	150	43	15
B91-97	500	200+150+150	9.9	150	43	15
B91-98	500	200+150+150	8.8	150	43	15
B91-99	500	200+150+150	13.2	150	43	15
B91-104	500+150+150	200	11	150	35	10
B91-105	500+150+150	200	11	150	35	5
B91-106	500+150+150	200	11	150	35	2
B91-107	25000	0	0	0	35	1

Table 2. **Doped quantum well superlattice APDs with spacer layer of 70A or 34A in each well and doping width variation with total dopant concentration constant.**

RUN #	L_b(A)	L_z(A)	Doping Density $10e^{17}cm^{-3}$	Doping Width Å	%Al Composition	Periods
B91-126	500	200+150+150+70	11	150	43	5
B91-127	500	200+150+150+34	11	150	43	5
B91-128	500	200+150+150+34	11	150	43	10
B91-129	500	200+150+150+70	11	150	43	10
B91-140	400	200+150+150+70	5	150	43	10
B91-143	500	300+100+100+70	7.5	100	43	10
B91-145	500	400+ 50+ 50+70	15	50	43	10
B91-146	500	450+ 25+ 25+70	30	25	43	10

Table 3. Summary of Current APD Performance Data.

MQW-APD	Doped Barrier MQW-APD	Doped Quantum Well MQW-APD
α/β = 1.7 - 2.5, for x = 0.30 = 2.5 - 3.3 for x = 0.43	α/β = 12.5 - 50, for $M_e \leq 5$ = 5 - 10, for $M_e > 5$-20	α/β = 10 - 50, for $M_e \leq 5$ = 5 - 10, for $M_e > 5$
Gains up to $M_e = 8$	Gains up to $M_e \approx 20$	Gains up to $M_e = 400$
Bias Voltages ≈ 70 - 90 V	Bias Voltages ≈ 6.5 - 9 V	Bias Voltages ≈ 9 - 14 V

2. Growth and characterization of HACT device materials:

As the starting point for this study we developed two structures for ACT device applications. The first was tailored according to a paper by Cullen [5], Tanski et.al [6]. A second structure was similar to the first one with a variation in Al mole fraction from 30% to 28% to minimize defects. Each structure was grown twice during different stages of MBE system operation. The characterization performed on these wafers has so far been limited to RHEED characterizations after growth to verify the crystallinity of the layers, a visual inspection of the surface for gross non-uniformity and surface particle density counts by Normarski microscopy. Hall effect measurements have also been performed to determine electrical properties.

The HACT structures were grown on high quality semi-insulating (100) GaAs wafers. During the initial heat treatment in the vacuum chamber, the substrate was baked at 380C for 4 hours. This was to remove water vapor and other atmospheric impurities from the moly holder and the substrate in the entry chamber. The substrate was subsequently transferred into the transition tube, where it resides at 10^{-9} Torr. After the growth rates and fluxes were set to appropriate values, the substrate was transferred into the growth chamber and arsenic and gallium oxides were thermally removed from its surface at 580C. The substrate was then subsequently baked at 640C under an arsenic over pressure for 45 minutes to remove any residual impurities. Growth was initiated using a 1000Å buffer layer of intrinsic GaAs to smoothen surface roughness, followed by a 25 period superlattice of 7 monolayer of AlGaAs and 5 monolayer of GaAs to block propagation of dislocations to the growth front.

Another buffer layer of 7500Å GaAs was grown to prepare a high quality surface before growing the first AlGaAs barrier of 1000Å. A 400Å undoped GaAs was then grown to form the 2DEG channel followed by 700Å of Si doped AlGaAs modulation doped layer. Finally a thin 200Å cap layer of i-GaAs was grown to protect the AlGaAs layer. A 30 second pause was used to interrupt the growth at each heterointerface. This allows the roughened growth surface to relax and become atomically smooth for the growth of subsequent AlGaAs layers. The sharpness of this interface is critical for the creation of a high quality 2DEG channel for charge transport.

To produce high performance HACT devices, the 2DEG channel should be free from any carriers and interfacial electron traps. Any electronic traps in the vicinity of the 2DEG channel will absorb carriers and hence deteriorate device performance. It is well known that AlGaAs has many deep electronic states known as D-X centers which capture carriers. Our approach has been to grow the AlGaAs doped with Si to an extent that saturates deep traps and interface states, while producing no additional free electrons. To accomplish this, based on prior experience we attempted doping the modulation doped layer at $2x10^{17}$ cm^{-3}. For this study the growth rates for GaAs were set at 0.5ML/SEC and at 0.214ML/sec for AlAs. The arsenic over pressure was $4.2x10^{-6}$ Torr. and the Si doping was set for $2x10^{17}cm^{-3}$ using GaAs calibration curves. The growth rates were determined by monitoring the RHEED intensity oscillations immediately prior to growth. Ga and As oxides were desorbed at T_{ox} = 555°C as read by the pyrometer which corresponds to 580°C, and the substrate was then baked for 2.5 hours at 640°C. After growth the measured surface particulate density was between 580 and 792 cm^{-2}. Hall measurement gave an electron concentration of $2.2x10^{17}cm^{-}$

^{3}, very close to the intended value of $2.0x10^{17}cm^{-3}$. This is very near the doping accuracy possible with MBE.

To calibrate the MBE system, and obtain a variety of samples for characterization, HACT structures with 28% Al in the modulation doped layer were also grown and doped at 2.0 to $7.2x10^{17}cm^{-3}$ for Hall evaluation. These samples are identical to the previous layers aside from the doping concentration in the AlGaAs layer. Next HACT structures were grown with AlGaAs layers which the thickness of the modulation doped layer, was varied from 350Å to 2100Å.

To obtain quick and relevant material characterizations we have also designed a semiconductor parameter test cell which will be incorporated into all HACT mask designs. This design includes structures for:

1. Schottky diodes for C-V and I-V measurements
2. Hall pattern for mobility and resistivity measurements
3. Transmission line contact resistance pattern for measuring sheet resistance and contact resistance
4. Large Schottky diode for DLTS measurements
5. Gate metal resistance pattern
6. Three short gate FET's
7. FATFET for mobility and transistor measurements

Also supporting characterizations such as

1. Photoluminescence spectroscopy
2. Fourier transform infrared spectroscopy

3. Mercury probe

4. Polaron (electrolytic) profiler

are available to support and supplement material investigations.

3. Charge transfer device:

During this period several designs were considered for testing the charge transfer device concept. The proposed structure consists of a GaAs n-p-n transistor grown by MBE in which the bottom n-type layer mimics the n-type contact of the APD and also becomes the well for charge storage. The p-type layer forms the barrier confining potential for the photo-multiplied electrons and can be removed by applying a large voltage to the top n^+-contact layer such that the electrons are injected into the top (ACT) layer. To form an overflow transistor it is proposed to remove part of the top n-type and to dope the surrounding and exposed p-type surface to a higher concentration by the ion-implantation of Be. The structure will be isolated by a proton implant and n- and p-type ohmic contacts deposited by conventional means. The detailed fabrication processes are currently being worked out and fabrication will commence next month.

4. Material growth improvements:

4.1 Development of Low-Defect Materials:

To improve material and surface quality we have implemented several new growth

techniques. First we have modified the Ga source to reduce Ga spitting, the cause of oval surface defects. Ga droplets condense near the top of the crucible, where the temperature is lower, and then roll back into the hot liquid Ga in the crucible and cause splashing. It is also possible that the Ga spheres formed near the top of the crucible explode and project Ga drops onto the GaAs growth surface. We have performed three modifications of the Ga source to reduce oval defect densities. The first involves using a PBN crucible coated with Al, as reported by Chand [7], and the second involves inserting an additional PBN sleeve into the Ga source, as reported by Maki et al. [8], to reduce the formation of Ga spheres. The third modification involved the installation of a two zone furnace, in which the crucible lip is separately heated.

To reduce surface particulate contamination we have designed a class 10 cleanroom glove box, with laminar flow, which will be attached to the wafer entry chamber of the MBE system. By preparing the wafers in this box we expect to significantly enhance our surface quality.

Finally, we have designed an indium free wafer holder to reduce the wafer handling process. These holders have been machined and are currently being tested. By removing the indium mounting from our pre- and post- growth processing, we expect to further reduce particle contamination on the surface and simplify the device fabrication process.

4.2 Precision doping techniques:

From the study of the APD device characteristics reported in the previous section it

became apparent that precise and equal n- and p-type doping was essential in order to optimize the total device structure. The cause of the observed imbalance in donor and acceptor doping is unknown at present but can be related to either material issues or system stability or a combination of both. Possible material issues involve the overlap of the donor and acceptor profiles either due to system error or surface segregation and diffusion and also for the doped quantum cell structures the diffusion of dopants from GaAs into the adjacent AlGaAs barrier. These material issues can cause both imbalances in the n- and p-type doping levels and of equal importance have a significant effect on the strength and profile of the bui. For this reason different doping techniques have been initiated as reported earlier. Also , SIMS studies of dopant profiles in device geometries where the co-presence of alu. could significantly affect the incorporation and diffusion rates from those expected in a simpler binary alloy such as GaAs. The use of other dopants such as carbon and lower growth temperatures could help to stabilize this situation. Additionally, p-i-n and delta-doping schemes which allow a clear separation of dopants will be investigated to both examine material issues and to explore the effect of different field profiles.

Of equal importance to these issues is the intrinsic accuracy of the MBE technique to grow these structures which require very accurate alloy and dopant concentrations and profiles. For this reason we have modeled the absolute precision that can be expected by doping MBE material using a conventional thermal source and a gas source, and also compared these results to the precision possible with a full CBE system.

For the doping variations in MBE grown GaAs both n- or p-type dopants substitute on

the Ga site and thus can be considered to form a very dilute alloy of the form $Ga_{1-x}D_xAs$. Because, the growth rate for GaAs is determined only by the Ga flux, then for elemental incorporation rates of R_D and R_{Ga} for the dopant and gallium atoms, respectively, the x-value becomes

$$x = \frac{R_D}{R_D + R_{Ga}} = \frac{R_D}{R_{Ga}} \tag{1}$$

for dopant concentrations $< 10^{19}cm^{-3}$, where $x < 10^{-3}$. For unhindered nucleation kinetics both incorporation rates are linear with flux giving

$$x = \frac{F_D}{F_{Ga}} \tag{2}$$

where F_D and F_{Ga} are now the element fluxes for the dopant and gallium. Since F_D and F_{Ga} are quite independent then the maximum variation in the x-value, δx is given by

$$\frac{\delta x}{x} = \sqrt{\left|\frac{\delta x}{x}\right|_D^2 + \left|\frac{\delta x}{x}\right|_{Ga}^2} = \sqrt{\left(\frac{\delta F}{F}\right)_D^2 + \left(\frac{\delta F}{F}\right)_{Ga}^2} \tag{3}$$

This formula can be used to estimate and compare the precision of MBE and CBE growth.

For MBE thermal Knudsen sources the flux is dependent on both the vapor pressure, P, of the element and the temperature, T, of the oven and is given by the following relationship

$$F \alpha \frac{P}{\sqrt{T}} \tag{4}$$

Because P and T are not independent variables then the variation in flux ΔF becomes

$$\frac{\Delta F}{F} = \frac{\Delta P}{P} - \frac{1}{2}\frac{\Delta T}{T} \tag{5}$$

and can be obtained directly from the vapor pressure relationships for Ga and the dopant, respectively. Substituting this equation in equation (3) then allows the dopant uniformity to be calculated.

For Si in GaAs we have:

$$\begin{aligned} \log(P_{Ga}) &= \frac{11{,}021.9}{T} + 7\log T - 15.42 \\ \log(P_{Si}) &= \frac{-18{,}588}{T} + 9.602 \end{aligned} \tag{6}$$

Also, for a growth rate of $\sim 0.5\mu$m (0.5ML/S) in the Varian GEN II system and a doping level of 10^{18}cm^{-3}, the Ga and Si oven temperatures are approximately 1100°C (1373K) and 1300°C (1573K), respectively. Assuming a temperature stabilization of $\Delta T = 0.5$K for each oven, the variation in the doping level as a function of the doping level has been calculated; where $\delta x/x = \delta N_D/N_D$.

For the CBE system we consider two situations 1) the use of a Si gas doping source during MBE growth, and 2) the doping accuracy with both CBE host and doping sources.

For the Si gas source the estimated stability of the flow controller system is 3.33×10^{-3}% at a doping level of $10^{18} cm^{-3}$. This estimate is obtained from similar experimental studies of the iodine doping of CdTe performed at GT. The Ga gas source stability was calculated assuming the flow controller was calibrated for 0.5μm/hr at 80% of full scale flow.

Figure 2 shows the results of these calculations for the various combinations of sources. As shown, the MBE Ga and Si sources give the highest variation in doping levels which decreases from 1.6% to 1.2% as the dopant concentration (oven temperature) is increased from 1×10^{15} to $> 1 \times 10^{18} cm^{-3}$. The combination of an MBE Ga source and a Si gas dopant source reduces the doping variation in the region of interest by a factor of 1.7. Since the dopant source is pressure controlled, as the flux (i.e., pressure) is reduced the relative instability increases for a given exit orifice size. At the higher doping levels, the stability is limited by the thermal stability of the Ga source.

The most favorable results are obtained by the use of both CBE Ga and Si sources. This further reduces the doping variation by an order of magnitude. This difference is directly attributable to the improvement in the stability of the Ga source. Again, the doping variation is limited by the Ga source at higher doping levels and the Si source at lower doping levels. However, by decreasing the conductance of the dopant source flow orifice it is possible to shift the stability curves to lower doping levels as indicated in the Figure. This is because it is possible to increase the dopant control pressure (and increase the relative stability) for a given doping level by reducing the flow orifice conductance.

It is quite significant that these calculations for the ideal operating conditions for MBE doping give an estimated accuracy of $\sim$ 1% which is within a factor of 5 - 10 of the doping

accuracy found in these structures. Consideration of the fact that the experimental observations are for balancing two dopant fluxes, and that there are also transient effects to be considered makes this analysis even more pertinent. Surprisingly, the main error is in the control possible over the Ga-flux which makes the CBE technique superior. However, the material issues mentioned previously must also be researched not only for their effect on the absolute doping accuracy but also because they will strongly impact the targeted field profiles that are required for optimum device performance.

REFERENCES

[1] Y. Kim and W.D. Hunt, "An analysis of surface acoustic wave propagation in a piezoelectric film over a GaAs/AlGaAs heterostructure," *Journal of Applied Physics*, vol. 71, no. 5, pp. 2136-2142, March 1992.

[2] W.D. Hunt, T. Cameron, J.C.B. Saw and Y. Kim, "Mode profiles in waveguide-coupled resonators," to be submitted to the *Journal of Applied Physics*.

[3] Y. Wang and K. F. Brennan, "k-dependence of the impact ionization transition rate in bulk InAs, GaAs, and Ge," *Journal of Applied Physics*, vol. 71, March 15, 1992.

[4] Aristin P., A. Torabi, A. K. Garrison, H. M. Harris and C. J. Summers, "New Doped Multiple-Quantum-Well Avalanche Photodiodes: The doped barrier $Al_{0.35}Ga_{0.65}As$/GaAs Multiple-Quantum-Well Avalanche Photodiode," *Appl. Phys.* Lett. 60, 85 (1992).

[5] Cullen, D. E., W. J. Tanski, S. W. Merritt, R. N. Sacks, R. D. Carroll, and E. J. Branciforte, *Ultrasonics Symposium 1988*, pp 135-143.

[6] Tanski, W. J., R. N. Sacks, S. W. Merritt, D. E. Cullen, E. J. Branciforte, T. C. Eschrich, and R. D. Carroll, *J. Vac. Sci. Technol.* B8 (2), 1990, pp 352-354.

[7] Chand, N., *J. Vac. Sci. Technol.*, B8 (2), 1990, pp 160-162.

[8] Maki, P. A., S. C. Palmateer, A. R. Calawa, and B. R. Lee, *J. Vac. Sci. Technol.* B4 (2), 1986, pp 564-567.

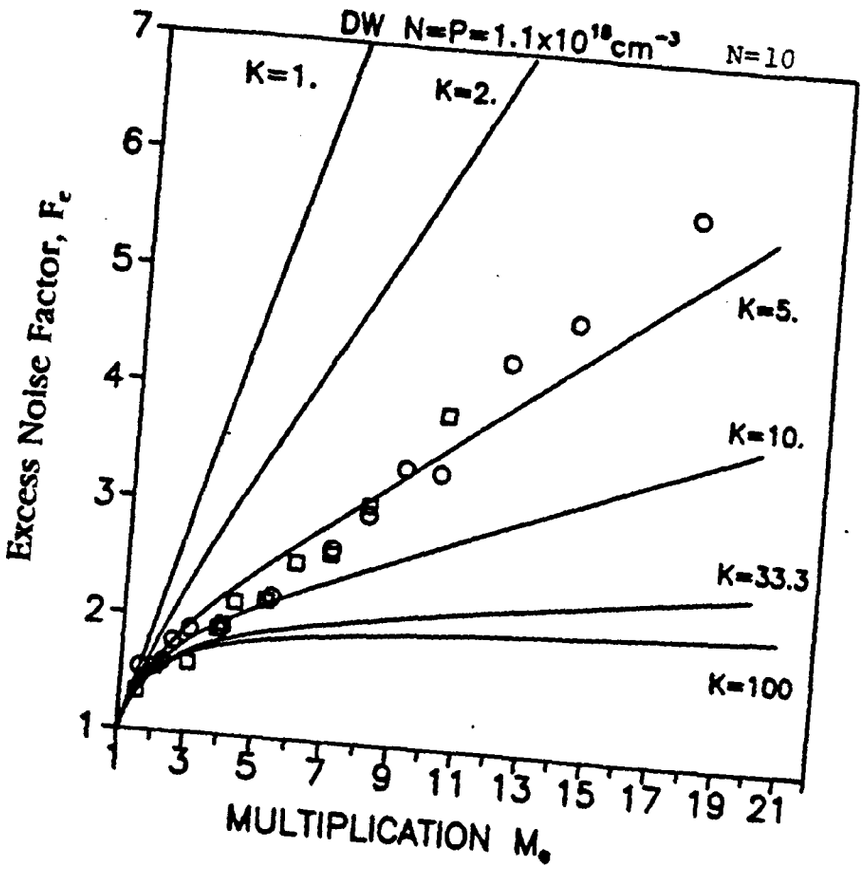

Figure 1. Excess noise factor, Fe, vs. gain, Me for doped quantum well APD.

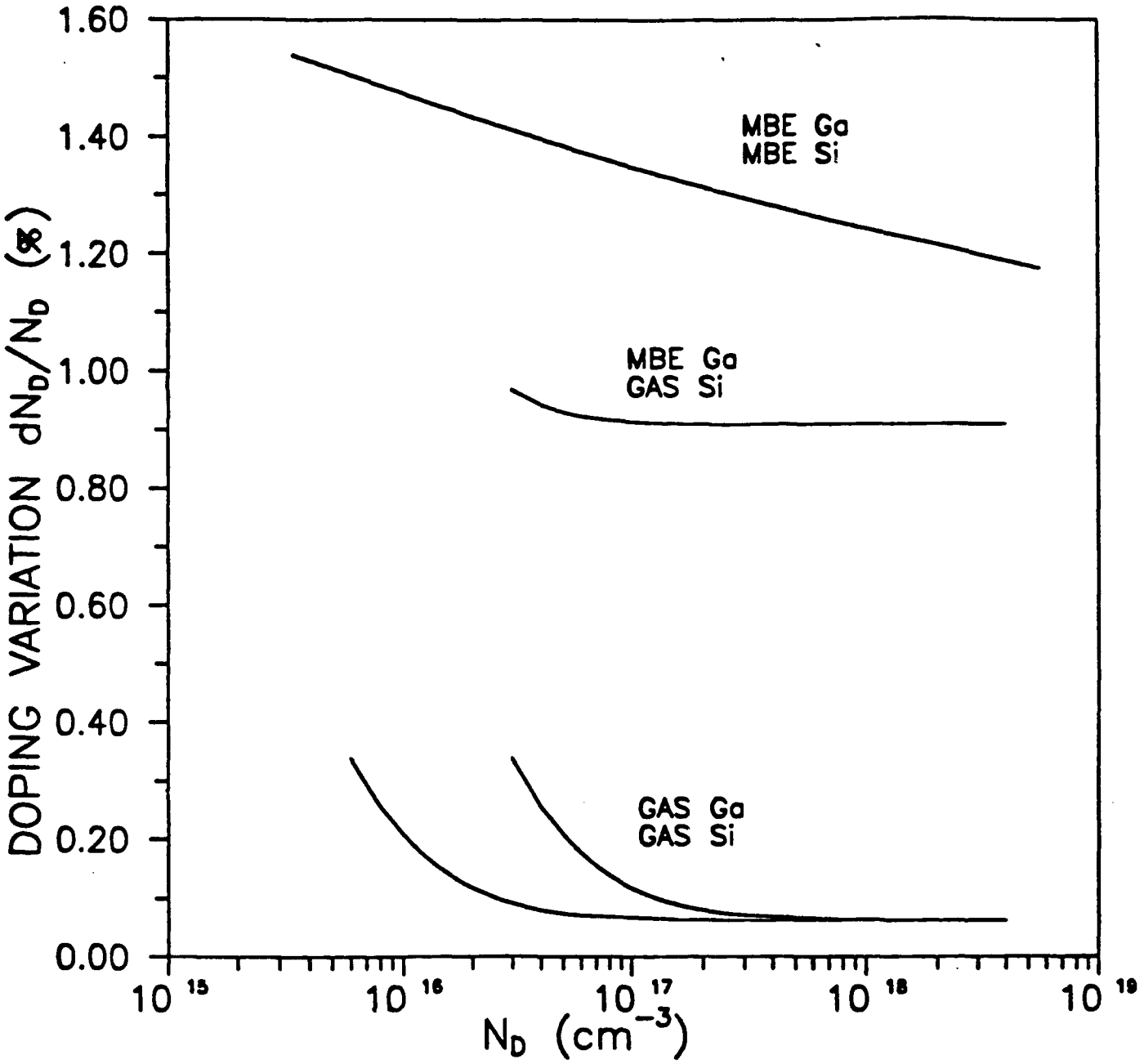

Figure 2. Doping variation vs. doping concentration for Si doped GaAs using conventional MBE thermal sources, gas source doping and CBE growth.